



VHL subgraph CFG integrated circuit ASAP scheduling

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The **common** shortcoming of heuristic techniques is a lack of optimality between the two steps of the (SAT)-based **scheduling** and binding approach, with a basic **ASAP/ALAP** De-embedding step. In other words, **scheduling** a DFG operation on a **CFG** edge is allowed when the two operations have the same **estimated start time**. Let us now describe the **integrated** flow in more detail. For the sake of readability, we will focus on the **binding** step.

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..... **subgraph** isomorphisms. In the second step (partitioning) **common** ancestor if they contain it. This graph will improve the **schedule** performances of the final architecture ...

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ment and system data-flow **subgraphs**, in order to identify the **common** components. The **allocation** is to be **integrated** in the **binding** step. The **scheduling** step is needed when **common** subcomponents shall be shared. Task ... and assigned component data-flow graph, **CFG** Particularly, the optimal **circuit** in relation to the area delay ...

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plication-specific **integrated circuit** (ASIC)]. As new processor architectures are When translating assembly codes from DSPs, it is **common** to encounter highly pipelined software the **subgraph** (**CFG**). Successive predicates form conjunctions. directed **scheduling** [41]. **ASAP** and **ALAP** **scheduling** gener- ...

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scale **integrated** (VLSIs) **circuits** become more and more important in the design Some systems separate DFG and **CFG**, others just combine both graphs. ... execution path or operation can be detected by traversing the **subgraph** between Both the **ASAP** and **ALAP** **scheduling** approaches stem out from unlimited ...

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ASAP and **ALAP** **scheduling** algorithms to determine the range of control steps Several **scheduling** techniques based on a control flow graph (**CFG**) model are ... for each variable in the loop, thus, resulting in a complex **sub graph** with a Today, Very High Speed

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a **common** approach in the design of embedded systems is to implement the control-dominated ... custom hardware, in application-specific **integrated-circuit** or field-programmable gate-array **subgraphs**. Finally, we apply standard Trimaran **scheduling** and **ASAP**, Steamboat Springs, CO, Sep. 2006, pp. 39–44. ...
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plexity of silicon-**integrated circuits** proceeds according to For the **CFG** and DFG some **common** basic properties (**ASAP**) driven, in other words, it is the simplest list scheduling execution time instead of rescheduling the task **subgraph**. By ... tended for combined retiming, **scheduling**, and partitioning ...
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maps high-level parallel C language descriptions into **circuit**- level netlists targeted to FPGAs. ... eral composed of three **subgraphs**, called the init, subunit and body graphs. that the **schedule** in the body graph is p2D1E to accommo- application representation, we **integrated** our findings seam- ...
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